Assignment of Folding Sets for Adaptive FIR Filtering on Folded Array

I. Milentijevic, V. Ciric
Faculty of Electronic Engineering, University of Nis, Serbia and Montenegro
{milentijevic,vciric}@elfak.ni.ac.yu

1. Introduction

The choice of structure for the implementation of an FIR filter includes consideration of the factors such as hardware complexity and throughput. Many different structures exist, most of which provide some trade-off between complexity and throughput [1,2]. For dedicated applications, the design choice then becomes the minimal complexity structure which can achieve a required throughput rate. The folding transformation is used to systematically determine the control circuits in DSP architectures where multiple algorithm operations are time multiplexed to a single functional unit [3]. By executing multiple algorithm operations on a single functional unit, the number of functional units in the implementation is reduced, resulting in integrated circuit with low silicon area [4]. As a starting architecture for the synthesis of the folded bit-plane FIR filter architecture with changeable folding sets, well-known bit-plane architecture (BPA) [5,6] was used in [7]. The BPA is highly regular architecture, which allows extensive pipelining, regular layout, high computational throughput, truncation of Least Significant Bits (LSBs) of intermediate results without any loss of accuracy, and programmability of coefficients [5,6]. Since the straightforward application of folding technique onto the BPA has not been possible, the transformation of the BPA data flow graph (DFG) that enables the synthesis of the folded FIR filter architecture has been proposed in [7]. That transformation allows the operation of FIR filter with changeable coefficient length, but with fixed number of coefficients. However, the problem of the designing of folded FIR filter with changeable number of coefficients still remains unsolved. The folding set assignment, described in [7], assumes that each node performs the same set of operations during the run time. That concept does not allow the synthesis of the FIR filter architecture with changeable number of coefficients. It is the reason why we propose a new assignment of folding sets where each node is capable of performing execution of any operation regardless to which folded set it belongs. The goal of this paper is to make synthesizing of folded architecture, which supports the changing of both coefficient number and coefficient length, possible. In order to enable the changing of coefficient number in fixed folded FIR filter array, we propose a new mapping of operations onto the DFG nodes rather then changing the topology of the DFG with additional transformations. The crucial novelty is that the new assignment enables the changing of operations in folding sets. In other words the different operations can be mapped onto the different hardware units in fixed array structure. The involving of changeable folding sets is aimed towards the increasing of versatility of folded bit-plane arrays.

2. Setting of Folding Sets

Transformation of the source DFG that enables the synthesis of the folded FIR filter architecture with changeable folding factor is given in [7]. This transformation allows the operation of FIR filter with changeable coefficient length, but with fixed number of coefficients. The architecture, described in [7] has an additional feature related on throughput increasing of folded system achieved through the reducing of folding factor according to the coefficient length. Our goal is the synthesis of folded architecture that will support the changing of both coefficient number and coefficient length. As a starting point in synthesis procedure we use the DFG that is a result of the transfer function transformation proposed in [7]. General transformed form of FIR filter transfer function, from [7], is

$$\begin{aligned} G(z) = {} & z^{0}\,(c_0^{m-1}2^{m-1} + c_0^{m-2}2^{m-2} + \ldots + c_0^{0}2^{0} + \\ & + z^{-1}\,(c_1^{m-1}2^{m-1} + c_1^{m-2}2^{m-2} + \ldots + c_1^{0}2^{0} + \\ & \ldots \\ & + z^{-1}\,(c_{k-1}^{m-1}2^{m-1} + c_{k-1}^{m-2}2^{m-2} + \ldots + c_{k-1}^{0}2^{0})\ldots). \end{aligned} \quad (1)$$

There are k folding sets, S_0, S_1, S_2, … ,S_{k-1}, and the number of folding sets is equal to tap number. Each folding set contains m operations, i.e. the folding factor N is equal to the coefficient length m_c. This manner of folding set assignment does not support the changing of number of taps. In order enable the changing of coefficient number in fixed folded FIR filter array we

propose a new mapping of operations onto the DFG nodes rather then changing the topology of the DFG with additional transformations. In order to explain setting of folding sets the following notation is involved:

m_c – coefficient length
k_c – number of coefficients
c_i^j – bit of coefficient c_i (with weight 2^j)
N – folding factor
k – number of folding sets
L – total number of "operations" in the DFG, where one operation assumes forming of partial product and the addition performed on one "row" of basic cells (basic cell contains AND gate and full adder)
p – position of operation within the DFG ($0 \le p \le L-1$)

An old assignment of following sets is done according to the following equations

$$s = \lfloor p / k_c \rfloor$$
$$r = p \bmod N. \quad (2)$$

This approach leads to the solution with changeable folding sets where the number of operations in folding set is changeable [7].

New assignment of folding sets ($S_S|r$) is involved with aim to enable the synthesis of the folded FIR filter architecture that will support the changing of both coefficient number and coefficient length. That feature is described with

$$s = p \bmod k$$
$$r = p \bmod N. \quad (3)$$

The crucial novelty is that (3) enables the changing of operations in folding sets. In other words the different operations can be mapped onto the different hardware units in fixed array structure. The equations (3) provide k folding sets where each folding set contains N operations. For the coefficients, k_c, and the coefficient length, m_c, the total number of operations, L, is:

$$L = k_c m_c = kN \quad (4)$$

Let us note that, the number of folding sets is not obligatory equal to the number of coefficients. In order to have the answer to the question whether the system is foldable or not, we have to calculate the folding equations and check the condition $D_f(U \to V) \ge 0$.

The folding equations can be given in the following form:

$$D_f(p \to p+1) = N \cdot w(e) - 0 + [(p+1) \bmod N] - [p \bmod N] =$$
$$= \begin{cases} -(N-1), & (p+1) \bmod N = 0 \\ N+1, & (p+1) \bmod m_c = 0 \\ 1, & otherwise \end{cases} \quad (5)$$

where $0 \le p \le L-2$. From (5), it can be seen that the condition $D_f(U \to V) \ge 0$ is not satisfied for neighboring nodes U and V when for the position p of node U the following is valid $p \bmod (N-1) = 0$ or $p \bmod N = 0$. This is the main reason for retiming of the DFG. Using the system of inequalities $D_f(U \to V) \ge 0$ and system of folding equations (5) the following system of inequalities in obtained

$$r(p) - r(p+1) \le \begin{cases} -1, & (p+1) \bmod N = 0 \\ 1, & (p+1) \bmod m_c = 0 \\ 0, & otherwise \end{cases},$$
$$for\ p = 0, 1, 2, \ldots, L-2. \quad (6)$$

The general form of solution for $r(p)$ is:

$$r(p) = \left\lfloor \frac{L-p}{m_c} \right\rfloor - \left\lfloor \frac{L-p}{N} \right\rfloor.$$

The existence of this solution provides the retiming of DFG and allows the application of folding technique. The new assignment of folding sets and solution for retiming are of great importance for the synthesis of folded FIR filter architecture that supports changing of number of taps and coefficient length.

3. Conclusion

New assignment of folding sets for the application of folding technique to the semi-systolic bit-plane FIR filter architecture is proposed in this paper. Mathematical description of folding set assignment is given with aim to enable the successful application of folding technique. The prerequisites for application of folding technique are satisfied. New assignment supports the changing of operations in folding sets. Using of proposed folding set assignment, different operations can be mapped onto the different hardware units in the fixed structure array.

4. References

[1] Robert Hawley, Bennett Wong, Thu-ji Lin, Joe Laskowski, Henry Samueli, "Design Techniques forr Silicon Compiler Implementations of High-Speed FIR Digital Filters", *IEEE Journal of Solid-State Circuits*, Vol 31, No. 5, May 1996.

[2] P. Corsonello, S. Perri, and G. Cocorullo, "Area-Time-Power Tradeoff in Cellular Arrays VLSI Implementations", *IEEE Transaction on Very Large Scale Integration (VLSI) Systems*, Vol. 8, No. 5, Oct. 2000, pp. 614-624.

[3] K.K. Parhi, VLSI Digital Signal Processing Systems (Design and Implementation), John Wiley & Sons, In., New York, 2000.

[4] T. C. Denk, K. K. Parhi, Synthesis of Folded Pipelined Architectures for Multirate DSP Algorithms, IEEE Transaction on Very Large Scale Integration (VLSI) Systems, Vol.6, No. 4, Dec. 1998, pp. 595-607.

[5] T. Noll, "Semi-systolic Maximum Rate Transversal Filters with Programmable coefficients", *Workshop of Systolic Architectures*, Oxford, 1986, pp. 103-112.

[6] D. Reuver, H. Klar, "A Configurable Convolution Chip with Programmable Coefficients", *IEEE Journal of Solid State Circuits*, Vol. 27, No. 7, July 1992, pp. 1121 -1123.

[7] I. Milentijevic, V. Ciric, O. Vojinovic, T. Tokic, "Folded Semi-Systolic FIR Filter Architecture With Changeable Folding Factor", *Neural, Parallel & Scientific Computations, Dynamic Publishers*, Atlanta, Vol. 10, No 2, 2002, pp. 235-247.